Divisie W&I, FEW
Vrije Universteit

Tentamen Computerorganisatie
7 Mei 2002

Voor Nederlands, z.o.z.

All 10 questions count equally. The midterm does not count.

1. Name three principles of RISC design.

2. A computer have a 5-stage pipeline. The clock speed is 1 GHz. In every clock cycle, each instruction shifts 1 stage verder in the pipeline. A new model has 10 stages and runs at 2 GHZ. How much faster is the new model than the old one?

3. Explain the concept of a superscalar architecture.

4. Draw a clocked SR latch.

5. A CPU has two caches, level 1 and level 2, with access times of 5 nsec and 10 nsec, respectively. The main memory has an access time of 50 nsec. If 20% of all the memory references are level 1 cache hits and 60% are level 2 cache hits, what is the average access time?

6. IJVM has a prefix 'WIDE'. What is it for?

7. The UltraSPARC has a register window to gain speed. Using a drawing, explain how it works.

8. A computer has a virtual memory with a page table that looks like this:

Virtual page	Physical page
0	2
1	-
2	0
3	8
4	-
5	1
6	3
7	4

Pages are 4 KB. Which physical address corresponds to each of the following virtual addresses: 9, 8193, 16383, 16384, 24000

9. An assembly language has both instructions and pseudoinstructions. Explain the difference between them.

10. (a) Is a NUMA machine a multiprocessor, a multicomputer, or something else?
(b) Explain how it differs from a UMA machine