Computer Systems Exam

24 March 2014

This is a closed book exam: no documentation is allowed. Please make sure that your handwriting is readable!

Q1. **(0.5 pt)** The following bitstring is the Hamming encoding of some initial data. Is it correct? And if not, which bit is wrong? Take for granted that no more than one bit may be wrong.

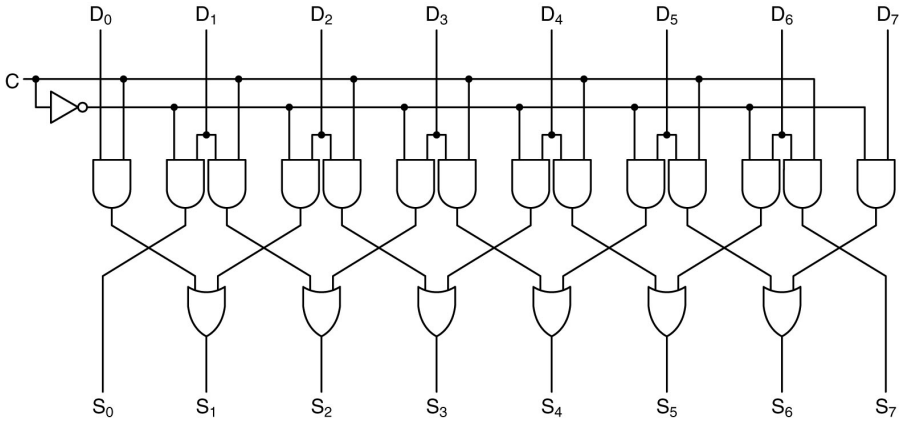
`0 0 0 1 1 1 0 0 0 1 1 1`

Q2. **(0.5 pt)** What was the revolutionary idea that the Von Neumann architecture introduced?

Q3. **(0.5 pt)** Draw a digital logic circuit which implements the following truth table. You can use only basic gates: AND, OR, NOT.

Input A	Input B	Input C	Output
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Q4. **(0.5 pt)** What does this circuit do? Explain briefly how it works.



Q5. **(1 pt)** Give the Java statement (e.g., `a=b+x`) that was translated to the following IJVM code:

```
ILOAD a
BIPUSH 45
ILOAD b
IADD
ISUB
ILOAD c
ILOAD d
IADD
DUP
IADD
ISUB
ISTORE x
```

Q6. **(0.5 pt)** Why are cache memories useful? What is the principle of their operation? (no details, just the principle)

Q7. **(0.5 pt)** The Mic-1 micro-instructions use 9 bits to select the registers where a micro-instruction's result must be stored, but only 4 bits to select the registers from which the operands must be read. Why?

Q8. **(1 pt)** What does the following micro-program do? Which IJVM instruction does it implement?

Main1	PC = PC + 1; fetch; goto (MBR)
xxx1	MAR = SP = SP - 1; rd
xxx2	MAR = SP = SP - 1
xxx3	H = MDR; rd
xxx4	OPC = TOS
xxx5	TOS = MDR
xxx6	Z = OPC - H; if (Z) goto T; else goto F

Q9. **(0.5 pt)** What is DMA (Direct Memory Access)? Why is it desirable?

Q10. **(1 pt)** A computer executes the following program:

```
int main () {
  int a, b, c;
  a = 10;
  b = 50;
  c = 267;
  foo(a);
  return 0;
}

void foo (int x) {
  int c, d;
  c = 30;
  d = 734;
  printf("%i\n", (c+d));
}
```

Show the complete content of the stack just *before* the `printf()` command is about to execute.

Q11. **(0.5 pt)** Draw the state-machine of a process (i.e., the diagram showing the possible states of a process, and the transitions among them).

Q12. **(0.5 pt)** A disk driver is using the **Shortest-Seek-Time-First** policy for ordering I/O requests. Currently the disk head is at zone 50, and the following I/O requests are pending. In which order will they be served?

- Read from zone 17
- Read from zone 92
- Write in zone 55
- Read from zone 48
- Write in zone 35
- Read from zone 80
- Read from zone 12

The disk arm is currently in front of block 50. Give the order in which the disk driver will process these requests. If there are multiple possible answers, give the full list of correct answers.

Q13. **(1 pt)** What does the TSL instruction do, and what advantages does it offer to process synchronization? Describe exactly the benefit(s) attributed to TSL, nothing less, nothing more. Describing additional benefits that are gained through *other* mechanisms will count against you ;-)

Q14. **(1 pt)** (a) What is an *interrupt*? (b) What is a *trap*? (c) What is the difference between them?

Q15. **(0.5 pt)** What is Virtual Memory, and why is it useful? Explain the principle (not details).

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