# Computer Systems Exam

25 March 2013

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**This is a closed book exam: no documentation is allowed. Please make sure that your handwriting is readable!**

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Q1. Encode the following word using Hamming code (with even parity):

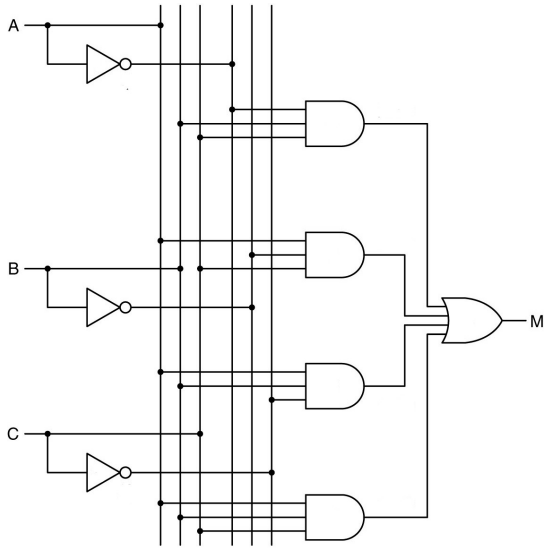
```
1 0 0 1 0 1 0 0 0 0 1 0 0 0
```

Q2. CPU frequencies have stopped increasing around year 2005. (a) Why did this happen? (b) Does this contradict Moore's law?

Q3. Draw a digital logic circuit which implements the following truth table. You can use only basic gates: AND, OR, NOT.

| Input A | Input B | Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Q4. What does this circuit do? Explain briefly how it works.



Q5. Give the Java statement (e.g., `a=b+x`) that was translated to the following IJVM code:

```
BIPUSH 5
ILOAD a
ISUB
ILOAD b
IADD
DUP
IADD
ISTORE x
```

Q6. (a) Explain the difference between a direct-mapped, a 2-way associative, and a 4-way associative CPU cache. (b) What are the advantages/disadvantages of direct-mapped and 4-way associative caches?

Q7. The Mic-1 micro-instructions use 9 bits to select the registers where a micro-instruction's result must be stored, but only 4 bits to select the registers from which the operands must be read. Why?

Q8. What does the following micro-program do? Which IJVM instruction does it implement?

| Main1 | PC = PC + 1; fetch; goto (MBR) |
|---|---|
| xxx1 | MAR = SP = SP - 1; rd |
| xxx2 | OPC = TOS |
| xxx3 | TOS = MDR |
| xxx4 | Z = OPC; if (Z) goto T; else goto F |

Q9. The Mic-1 allows a register's value to be fed to the ALU, an arithmetic operation to be performed, and the results to be written back to the same register in a single clock cycle (e.g., `SP = SP - 1`). Why doesn't reading from and writing to the same register in a single clock cycle cause trouble?

Q10. Current modern CPUs use pipelines with 7 to 10 stages. Explain why adding more stages will not necessarily improve performance.

Q11. What is DMA (Direct Memory Access)? Why is it desirable?

Q12. A computer executes the following program:

```
int main () {
  int a, b;
  a = 8;
  b = 4;
  foo(a);
  return 0;
}

void foo (int x) {
  int c = 5;
  c = c+x;
}
```

Show the content of the stack while function `foo()` is executing (i.e., at line "`c=c+x;`").

Q13. (a) What does the TSL instruction do? (b) Why it is useful for implementing process synchronization?

Q14. What is the result of this reverse polish notation computation?
`7 3 - 10 2 5 * / *`

Q15. Draw the state-machine of a process (i.e., the diagram showing the possible states of a process, and the transitions among them).

Q16. A disk driver is using the Scan policy for ordering I/O requests. In the recent past it has received the following list of requests that it didn't have time to serve:

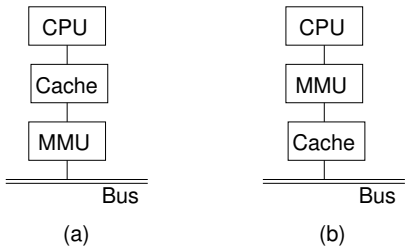
- Read block 122
- Read block 83
- Read block 201
- Write block 71
- Read block 10
- Write block 0
- Write block 92
- Read block 500

The disk arm is currently in front of block 500. Give the order in which the disk driver will process these requests. If there are multiple possible answers, give the full list of correct answers.

Q17. Explain what is a race condition. What can be done about it?

Q18. Virtual memory pages usually have a size which is a power of 2 (for example: 2048 bytes). Could we decide instead to have page sizes which are not a power of 2, such as 4000 bytes per page? What should we change in our computer architecture design to support such a page size?

Q19. Between a CPU and its bus, there are two intermediate elements: the MMU and the L1 cache. Which of the following two designs is correct? Explain why.




Q20. How are the ISA and Micro-programming languages related?

**— the end —**