Chapter 10 – Computer Peripherals

10.1. *Revised problem statement:* The total time required to illuminate each pixel on the display screen of a computer monitor is 5ns. The beam is then turned off and moved to the next point to be illuminated. On average, moving the beam from one spot to the next takes 12 ns. What is the maximum possible resolution of this display if it is to be refreshed 70 times per second.

For *N* pixels we get

$$\text{Scan time} = (5 + 12)N = 10^9/70 = 14.3\text{ns}$$

Hence,*N* = 840000 pixels

A commercial standard that would not exceed this resolution is 1024×768.

10.2. Each symbol can have one of eight possible values, which means it represents three bits. Therefore:

$$\text{Bit rate} = 3 \times \text{baud rate} = 3 \times 9600 = 28,800\ \text{bits/s}$$

10.3. In preparing this design we have assumed the following:

- The counter has a synchronous Clear signal. That is, the counter is cleared to 0 on the clock edge at the end of a clock period during which Clear = 1.
- The shift register has a synchronous control signal called Shift. The data value at its serial input is shifted into the register on the clock edge at the end of a clock period during which Shift = 1.

We use a D flip-flop as a synchronizer for the input data. Its output, SData, follows the input data, but is synchronized with the local clock. It is connected to the serial input of the shift register. Both the shift register and the counter are driven by the local clock.

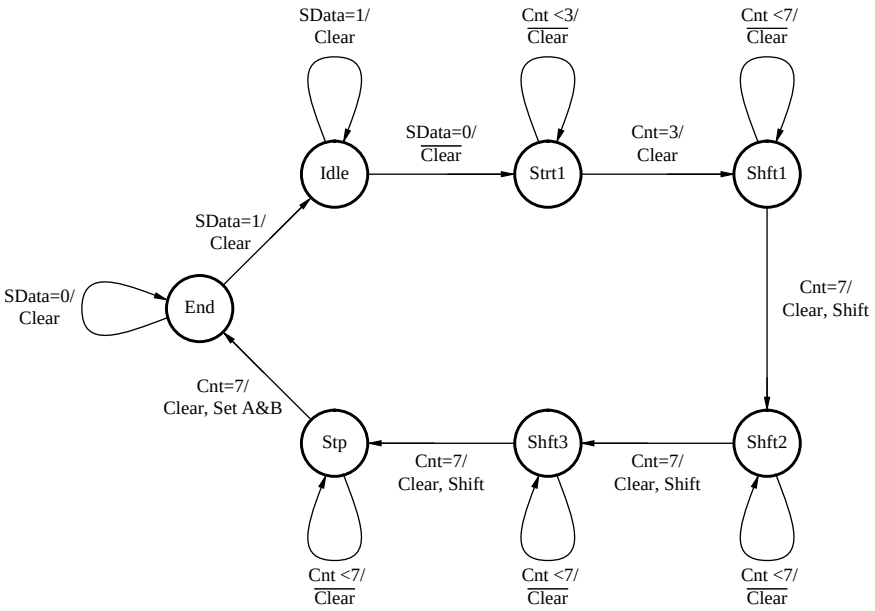
We will now describe the control logic that generates the Clear and Shift signals. Starting from an idle state in which SData = 1, Clear = 1, and Shift = 0, the sequence of events that the control logic needs to implement is as follows:

(a) When SData = 0 change Clear to 0. The counter starts to count.

(b) When count = 3 (the fourth clock cycle), set Clear = 1 for one clock cycle. The clock edge at the end of this cycle is the mid-point of the Start bit. The counter is cleared to 0 at this point, then it starts to count again.

(c) When count reaches 7, set both Clear and Shift to 1 for one clock cycle. At the end of this clock cycle, the first data bit is loaded in the shift register and the counter is again cleared to 0. Repeat twice.

(d) When count = 7, set A = SDATA and B = $\overline{\text{SData}}$.



(e) Wait until SData = 1 then return to step 1.

A state diagram for the control logic is given below. When not specified, outputs are equal to zero.

10.4 Each data byte requires 10 bits to transmit. Hence, the effective transmission rate is 38,800/10 = 3,800 bytes/s.

10.5 A: 1100 0001, P: 0101 0000, =: 0011 1101, 5: 1011 0101

10.6 *(Correction: Bit b_7 is the Data Set Ready signal, CC).*

We will refer to the register given in the problem as STATUS. The program below deals with an incoming call.

```
        BitSet    #1,STATUS     Enable automatic answering
RING    BitTest   #14,Status    Wait for ringing signal
        Branch=0  RING
* At this point, the program may alert the user (or the operating-system) of an in-coming call
Ready   BitTest   #7,Status     Wait for Data Set Ready
        Branch=0  Ready
        BitSet    #2,STATUS     Enable send carrier
SENDC   BitTest   #13,STATUS    Wait for confirmation
        Branch=0  SENDC
RECVC   BitTest   #12,STATUS    Wait for receive carrier
        Branch=0  RECVC
* Program is now ready to send and receive data
```